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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/462,994    01/14/00    SCHWALKE

U    P99.2666

EXAMINER

MMC2/0713

SCHIFF HARDIN & WHITE  
PATENT DEPARTMENT  
7100 SEARS TOWER  
CHICAGO IL 60606-6473

KEBEDE, D  
ART UNIT

PAPER NUMBER

2823  
DATE MAILED:

07/13/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trad marks**

<b>Office Action Summary</b>	Application No. 09/462,994	Applicant(s) SCHWALKE ET AL.	
	Examiner Brook Kebede	Art Unit 2823	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 January 2000.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

- |   |  |
|---|--|
| 15) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                  | 18) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 16) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)         | 19) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 17) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 20) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Priority***

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Paper No. 1 on January 4, 2000. It is noted, however, that applicant has not filed a certified copy of the original application as required by 35 U.S.C. 119(b).

### ***Oath/Declaration***

2. A new oath or declaration is required because the title should be in English. The wording of an oath or declaration cannot be amended. If the wording is not correct or if all of the required affirmations have not been made or if it has not been properly subscribed to, a new oath or declaration is required. The new oath or declaration must properly identify the application of which it is to form a part, preferably by application number and filing date in the body of the oath or declaration. See MPEP §§ 602.01 and 602.02.

### ***Specification***

3. The abstract of the disclosure is objected to because the recitation "Figure 6" in line 8 is not clear. Correction is required. See MPEP § 608.01(b).

4. The specification is objected because the recitation "[sic]" in page 1, line 24 and in page 4, line 18 is not clear.

### ***Claim Rejections - 35 USC § 112***

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Art Unit: 2823

6. Claims 8-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In the method claim, at least one positive (active) step must be recited in the claimed invention. Regarding claim 8, none of the claimed limitations have a positive step.

For instance, the limitation in claim 8, lines 1-10, "Method for manufacturing an integrated circuit arrangement, whereby a doped region (3) is formed in a semiconductor substrate (1); whereby a plane having conductive useful structures (71) and at least one conductive filler structure (72) is formed on the semiconductor substrate (1) by application and structuring of a conductive layer (7); whereby an insulation layer (11, 12) is produced that surrounds and covers the conductive useful structures (71) and the conductive filler structure (72); whereby a conductive connection is produced between the conductive filler structure (72) and the doped region (3)." does not provide any active element that establish the claimed invention is a method (process) claim. As best understood the recited claim limitation, in claim 8 and consecutive claims, is a product-by-process claim. As a result it is difficult for the Examiner to determine what actually applicants are intended to claim, i.e., process or product. Therefore, it renders the claim indefinite in its scope.

Claims 9 and 10 also rejected for the same reason as described herein above and as being dependent of the rejected independent base claim.

7. Applicants' cooperation is requested in reviewing the claims structure to ensure proper claim construction and to correct any subsequently discovered instances of claim language noncompliance. See *Morton International Inc.*, 28USPQ2d 1190, 1195 (CAFC, 1993).

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

9. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Uehara et al. (US/5,698,902).

Re claim 1, Uehara et al. disclose an integrated circuit arrangement having at least one doped region (21 21a 21b) is provided in a semiconductor substrate (10); having a plane with conductive useful structures (50a) (i.e. a gate electrode) and at least one conductive filler structure (50b) is arranged at the surface of the semiconductor substrate (10); whereby the conductive filler structure (50b) is conductively connected to the doped region (21) (see Fig. 6).

Re claim 2, as applied to claim 1 above, Uehara et al. disclose all the claimed limitation including the limitation whereby the conductive useful structures (50a ) and the conductive filler structure (50b) exhibit essentially the same height and are surrounded by a planarizing insulation layer (32) (see Fig. 6).

Re claim 3, as applied to claim 1 or 2 above, Uehara et al. disclose all the claimed limitation including the limitation whereby the conductive filler structure (50b) is connected to the doped region (21) via a via hole and a contact (i.e. the contact used to form withdrawn electrode (31) (not labeled) (see Fig. 6).

Re claim 4 as applied to claim 3 above, Uehara et al. disclose all the claimed limitation including the limitation whereby the via hole overlaps the conductive filler structure (50b) and the doped region (21), so that the surface of the conductive filler structure (50b) and of the doped region (21) are in communication with the contact (i.e. withdrawn electrode) (31) (see Fig. 6).

Re claim 5, as applied to one of the claims 1-4 above, Uehara et al. disclose all the claimed limitation including the limitation whereby the conductive useful structures (50a) are gate electrodes and whereby the conductive filler structure (50b) contains the material of the gate electrode (see Fig. 6).

Re claim 6, as applied to one of the claims 1-5 above, Uehara et al. disclose all the claimed limitation including the limitation whereby the doped region (21) is a doped well or the semiconductor substrate (10) (see Fig. 6).

Re claim 7, as applied to one of the claims 1-6 above, Uehara et al. disclose all the claimed limitation including the limitation whereby a metallization level (34) is arranged above the plane wherein the conductive filler structure (50b) is arranged; whereby the conductive filler structure (50b) is connected to the metallization level (34) via a further contact (i.e. the contact a buried layer (33) is formed) (not labeled) (see Fig. 6)

Re claim 8, Uehara et al. disclose a method for manufacturing an integrated circuit arrangement, whereby a doped region (21) is formed in a semiconductor substrate (10); whereby a plane having conductive useful structures (50a) and at least one conductive filler structure (50b) is formed on the semiconductor substrate (10) by application and structuring of a conductive layer (15b 16b); whereby an insulation layer (32) is produced that surrounds and covers the conductive useful structures (50a) and the conductive filler structure (50b); whereby a

conductive connection is produced between the conductive filler structure (50b) and the doped region (21) (see Fig. 6).

Re claim 9, as applied to claim 8 above, Uehara et al. disclose all the claimed limitations including whereby a via hole is opened in the insulation layer (32), said via hole respectively partially overlapping the conductive filler structure (50b) and the doped region (21), so that the surface of the doped region (21) and of the conductive filler structure (50b) is partially uncovered; whereby a contact (31) is formed in the via hole (not labeled), said contact being in communication with the surface of the conductive filler structure (50b) and of the doped region (21) (see Fig. 6).

Re claim 10, as applied to claim 8 or 9, Uehara et al. disclose all the claimed limitations including whereby a metallization level (34) is produced above the plane wherein the conductive filler structure (50b) is arranged; whereby a further contact (33) is produced via which the conductive filler structure is connected to the metallization level (34) (see Fig. 6).

### ***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Misra et al. (US/5,960,270), Masuoka (US/5,994,197), Asamura (US/6,074,938), Teo et al. (US/6,204,137) and Erdeljic et al. (US/6,236,101).

### ***Correspondence***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

Art Unit: 2823

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

13. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede

*BK*  
July 11, 2001



Trung Dang  
Primary Examiner